UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,391	01/23/2004	Melany Ann Richmond	ZIL-555	8983

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EXAMINER
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ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/764,391	RICHMOND ET AL.
	Examiner	Art Unit	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL.**   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

This Office Action is sent in response to Applicant's Communication received July 10,

2006 for application number 10/764391 originally filed January 23, 2004. The Office hereby

5   acknowledges receipt of the following and placed of record in file: amended claims 1-23 wherein

claims 22 and 23 are new.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

10   basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on
> sale in this country. more than one year prior to the date of application for patent in the United States.

15   Claim 19 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bongiorno et

al. (U.S. Patent No. 6,292,045 B1) (hereinafter referred to as Bongiorno).

As to claim 19, Bongiorno discloses a microcontroller integrated circuit (100) operable

with an external first clock circuit (10), the microcontroller integrated circuit (column 1, lines 10-

39) comprising: (a) a processor (80) having a system clock input lead (it is inherent in the art that

20   a processor chip will have a system clock input lead; column 4, lines 2-8); (b) a terminal

(element 100 is noted as an "inventive circuit" which necessitates a terminal to receive the clock

from circuit 10; column 3, lines 52-57) for receiving a first clock signal (via 10) generated by the

external first clock circuit (10) (column 4, lines 1-8); (c) a second clock circuit (20); and (d)

means for detecting (40; figs. 1A and/or 1B) whether the first clock signal (10) is inadequate

(checks to see if clock signal is available; column 4, lines 22-27) and, upon detecting that the

first clock signal is inadequate (via timer 70; column 4, lines 8-21), for decoupling (deselecting

via switching means 66 within 60) the terminal from the system clock input lead and coupling

(selecting via switching means 66 within 60) the second clock circuit (20) to the system clock

5   input lead, wherein the means decouples (deselects) the terminal from the system clock input

lead and couples the second clock circuit (20) to the system clock input lead without receiving

any signal from the processor (Bongiorno discloses a clock selection circuit wherein a timer [70]

that can be a separate circuit from the microprocessor [80] and detects a first clock circuit [10] is

inadequate [malfunctioning], deselects the first clock [10] via switching means [66 within 60]

10   and selects and second clock circuit [20] also using the switching means; column 4, lines 9-34

and column 4, line 61 thru column 5, line 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

15   obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
20 > manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

25   1.   Determining the scope and contents of the prior art.
         2.   Ascertaining the differences between the prior art and the claims at issue.

3.   Resolving the level of ordinary skill in the pertinent art.

4.   Considering objective evidence present in the application indicating obviousness or nonobviousness.

5   Claims 1-7, 9-18 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Bongiorno et al. (U.S. Patent No. 6,292,045 B1) (hereinafter referred to as Bongiorno) in

view of Kemeny et al. (U.S. Patent No. 7,062,675 B1) (hereinafter referred to as Kemeny).

As to claim 1, Bongiorno discloses a method comprising: (a) detecting (via 50) whether a

first clock signal (from clock source 10) is inadequate (checks to see if clock signal is available),

10   wherein the first clock signal is generated by a first clock circuit (column 4, lines 22-27); (b)

decoupling (deselecting via switching means 66 within 60) the first clock circuit (10) from a

system clock input lead of a processor, wherein the decoupling is not performed as a result of a

signal from the processor (Bongiorno discloses a malfunctioning clock signal being deselected

[via switching means 66 within 60] from a processor [80] after watchdog timer [70] sends out a

15   reset signal to the processor; therefore decoupling is performed as a result of the timer [70] and

not the processor; column 4, lines 9-21 and column 4, line 61 thru column 5, line 7); (c) coupling

(selecting) a second clock circuit (20) to the system clock input lead of the processor (Bongiorno

discloses a second clock circuit [20] being selected [via switching means 66 within 60] to the

processor[80]; column 4, lines 2-8 and column 4, lines 22-34 and column 4, line 61 thru column

20   5, line 7); (e) decoupling (deselecting) the second clock circuit (20) from the system clock input

lead of the processor (Bongiorno discloses the malfunctioning clock signal being deselected [via

switching means 66 within 60] from a processor [80]; column 4, line 61 thru column 5, line 7);

and (f) coupling (selecting) a third clock circuit (30) to the system clock input lead of the

processor (Bongiorno discloses a third clock circuit [30] being selected [via switching means 66

within 60] to the processor[80]; column 4, lines 2-8 and column 4, lines 22-34 and column 4, line 61 thru column 5, line 7).

Bongiorno fails to disclose the method comprising the step: (d) enabling a third clock circuit.

5   Kemeny teaches a cache system comprising a shutdown scheme wherein when a detection logic (32) detects loss of power a backup power supply (30) is turned on when the failure is detected (column 4, lines 45-51). Kemeny has the additional feature of providing a reliable cache flushing system to prevent system failure when a power loss is detected (column 1, lines 58-67).

10   It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Kemeny at the time the invention was made, to modify the clock switching method of Bongiorno to include the ability to enable (power on) back-up circuits when the primary fail is detected as taught by Kemeny such that when a primary clock fails the back-up replacement clock is enabled (powered-on) before use. One of ordinary skill in the art would be

15   motivated to make this combination of enabling/powering back-up circuits when needed after detecting a failure of a primary circuit in view of the teachings of Kemeny, as doing so would give the added benefit of providing a reliable cache flushing system to prevent system failure when a power loss is detected (as taught by Kemeny above).

As to claim 2, Bongiorno in combination with Kemeny taught the method in claim 1, as

20   shown above. Bongiorno further teaches the method wherein the first clock circuit a high-speed, external crystal oscillator, wherein the second clock circuit is a low-speed, internal watchdog timer, and wherein the third clock circuit is a high-speed, internal oscillator (Bongiorno discloses

a clock circuit having the ability to comprise various types of both internal and external clock

sources that can be any combination of such as a crystal oscillator, a crystal resonator, a

complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator

[as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC)

5   oscillator; column 1, lines 10-39).

As to claim 3, Bongiorno in combination with Kemeny taught the method in claim 1, as

shown above. Bongiorno further teaches the method wherein the detecting is performed by

detecting no signal edges of the first clock signal during a time period over which a linear

feedback shift register increments to a predetermined value (Bongiorno discloses the timer

10   monitoring the processor clock signal such that a predetermined count value [pre-set time-out

period] is incremented, as is known in the art, which can be done with or without an LFSR;

column 1, lines 26-39).

As to claim 4, Bongiorno in combination with Kemeny taught the method in claim 1, as

shown above. Bongiorno further teaches the method wherein the second clock circuit generates a

15   signal whose frequency is lower than that of the first clock signal, and wherein the second clock

circuit and the processor are parts of a single integrated circuit (column 1, lines 11-25).

As to claim 5, Bongiorno in combination with Kemeny taught the method in claim 1, as

shown above. Bongiorno further teaches the method wherein the coupling the second clock

circuit in (c) is not performed as a result of a signal from the processor (Bongiorno discloses a

20   malfunctioning clock signal being deselected from a processor after watchdog timer sends out a

reset signal to the processor; therefore decoupling is performed as a result of the timer and not

the processor; column 4, lines 9-21 and column 4, line 61 thru column 5, line 7).

As to claim 6, Bongiorno in combination with Kemeny taught the method in claim 1, as shown above. Kemeny further teaches the method wherein the third clock circuit is enabled in (d) by powering up the third clock circuit (column 3, lines 8-20).

As to claim 7, Bongiorno in combination with Kemeny taught the method in claim 1, as

5 shown above. Bongiorno further teaches the method further comprising, between step (a) and step (b): sending an interrupt signal (reset signal) to the processor indicating that the first clock circuit has failed (column 4, lines 9-21).

As to claim 9, Bongiorno in combination with Kemeny taught the method in claim 1, as shown above. Bongiorno further teaches the method further comprising, between step (d) and

10 step (e): (g) detecting (via detector 50) whether a second clock signal is inadequate, wherein the second clock signal is generated by the third clock circuit (Bongiorno discloses the detector circuit [50] detecting the availability of the clocks that are selected; column 4, lines 22-38).

As to claim 10, Bongiorno in combination with Kemeny taught the method in claim 1, as shown above. Bongiorno further teaches the method wherein the first clock circuit can be

15 coupled to the system clock input lead by a multiplexer, the first clock circuit being coupled to a first data input lead of the multiplexer, wherein the second clock circuit is coupled in (c) to the system clock input lead by the multiplexer, the second clock circuit being coupled to a second data input lead of the multiplexer, wherein a third data input lead of the multiplexer is grounded (inherently grounded as all circuits are grounded), and wherein between step (b) and step (c) the

20 multiplexer couples the third data input lead of the multiplexer to the system clock input lead (column 4, line 61 thru column 4, line 7).

As to claim 11, Bongiorno discloses an integrated circuit, comprising: (a) a processor

(80) with a system clock input lead (it is inherent in the art that a processor chip will have a

system clock input lead; column 4, lines 2-8); (b) a terminal (element 100 is noted as an

"inventive circuit" which necessitates a terminal to receive the clock from circuit 10; column 3,

5   lines 52-57), the terminal coupled to a first clock circuit (10), the first clock circuit generating a

first clock signal (column 4, lines 1-8); (c) a second clock circuit (20); (d) a third clock circuit

(30); and (e) a clock controller (40) coupled to the system clock input lead (figs. 1A and/or 1B;

column 4, lines 2-15), wherein the clock controller is adapted to decouple (deselect via switching

means 66 within 60; Bongiorno discloses a failing clock signal [detected by timer 70] being

10   deselected [via switching means 66 within 60] from a processor [80]; column 4, lines 9-34) the

system clock input lead from the terminal and to couple (select via switching means 66 within

60; Bongiorno discloses another clock signal being selected [via switching means 66 within 60]

to the processor[80] when one delivered has failed [times out as detected by timer 70]; column 4,

lines 2-34 and column 4, line 61 thru column 5, line 7) the system clock input lead to the second

15   clock circuit (20) upon detecting that the first clock signal has failed (timed out), and wherein the

clock controller is further adapted to select the third clock circuit (30) upon detecting that the

first clock signal has failed (Bongiorno discloses a third clock circuit [30] being selected [via

switching means 66 within 60] to the processor[80]; column 4, lines 2-34 and column 4, line 61

thru column 5, line 7) (Bongiorno further teaches that "failure" has been detected when timer

20   [70] detects [by a time-out period] a "control failure or a lockup" which, as earlier shown in

Bongiorno, comprises a clock failure; column 1, lines 26-39 and column 4, lines 11-17).

Bongiorno fails to disclose the clock controller is adapted to turn on the third clock circuit.

Kemeny teaches a cache system comprising a shutdown scheme wherein when a detection logic (32) detects loss of power a backup power supply (30) is turned on when the

5   failure is detected (column 4, lines 45-51). Kemeny has the additional feature of providing a reliable cache flushing system to prevent system failure when a power loss is detected (column 1, lines 58-67).

It would have been obvious to one of ordinary skill of the art having the teachings of Bongiorno and Kemeny at the time the invention was made, to modify the clock switching

10   method of Bongiorno to include the ability to enable (power on) back-up circuits when the primary fail is detected as taught by Kemeny such that when a primary clock fails the back-up replacement clock is enabled (powered-on) before use. One of ordinary skill in the art would be motivated to make this combination of enabling/powering back-up circuits when needed after detecting a failure of a primary circuit in view of the teachings of Kemeny, as doing so would

15   give the added benefit of providing a reliable cache flushing system to prevent system failure when a power loss is detected (as taught by Kemeny above).

As to claim 12, Bongiorno discloses the integrated circuit wherein the first clock circuit is a high-speed external crystal oscillator (Bongiorno discloses a clock circuit having the ability to comprise various types of both internal and external clock sources that can be any combination

20   of such as a crystal oscillator, a crystal resonator, a complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator [as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC) oscillator; column 1, lines 10-39).

As to claim 13, Bongiorno discloses the integrated circuit wherein the second clock

circuit is a low-speed, internal watchdog timer (column 4, lines 9-15) oscillator (Bongiorno

discloses a clock circuit having the ability to comprise various types of both internal and external

clock sources that can be any combination of such as a crystal oscillator, a crystal resonator, a

5   complementary metal-oxide semiconductor (CMOS) clock, a resistor-capacitor (RC) oscillator

[as is known in the art to be a slow, low-power clock source] and an inductor-capacitor (LC)

oscillator; column 1, lines 10-39).

As to claim 14, Bongiorno discloses the integrated circuit wherein the clock controller

can decouple the system clock input lead from the terminal when the processor is receiving an

10   inadequate first clock signal (column 1, lines 11-25).

As to claim 15, Bongiorno discloses the integrated circuit wherein the clock controller

decouples the system clock input lead from the second clock circuit and couples the system clock

input lead to the third clock circuit (column 3, lines 8-20).

As to claim 16, Bongiorno discloses the integrated circuit wherein the clock controller

15   comprises a primary clock source fail detect circuit (51), and wherein the primary clock source

fail detect circuit detects whether the first clock signal has failed (is available) (column 5, lines

29-52).

As to claims 17 and 18, they are directed to the integrated circuit of steps set forth in

claim 16. Therefore, they are rejected for the same basis as set forth hereinabove.

20   As to claim 22, Bongiorno in combination with Kemeny taught the method in claim 1, as

shown above. Bongiorno further teaches the method wherein the second clock circuit is a low-

power, RC oscillator (column 1, lines 11-25).

As to claim 23, Bongiorno in combination with Kemeny taught the method in claim 1, as

shown above. Bongiorno further teaches the method wherein the third clock circuit is entirely

on-chip and does not have an external crystal (column 1, lines 11-25).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno (as

5   cited above) as applied to claim 19 above, and further in view of Kemeny (as cited above).

Bongiorno fails to disclose the clock controller is adapted to turn on the third clock

circuit.

Kemeny teaches a cache system comprising a shutdown scheme wherein when a

detection logic (32) detects loss of power a backup power supply (30) is turned on when the

10   failure is detected (column 4, lines 45-51). Kemeny has the additional feature of providing a

reliable cache flushing system to prevent system failure when a power loss is detected (column 1,

lines 58-67).

It would have been obvious to one of ordinary skill of the art having the teachings of

Bongiorno and Kemeny at the time the invention was made, to modify the clock switching

15   method of Bongiorno to include the ability to enable (power on) back-up circuits when the

primary fail is detected as taught by Kemeny such that when a primary clock fails the back-up

replacement clock is enabled (powered-on) before use. One of ordinary skill in the art would be

motivated to make this combination of enabling/powering back-up circuits when needed after

detecting a failure of a primary circuit in view of the teachings of Kemeny, as doing so would

20   give the added benefit of providing a reliable cache flushing system to prevent system failure

when a power loss is detected (as taught by Kemeny above).

As to claim 21, it is directed to the integrated circuit of steps set forth in claim 20.

Therefore, it is rejected for the same basis as set forth hereinabove.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bongiorno and

Kemeny as applied to claim 1 above, and further in view of Ohlenbusch et al. (U.S. Patent

5   Publication No. 2002/0091785 A1) (hereinafter referred to as Ohlenbusch).

Neither Bongiorno nor Kemeny teach disabling a detection circuit.

Ohlenbusch teaches an intelligent data network wherein devices that are unnecessary are

turned off so as save power in the system (paragraph 36, lines 11-16). Ohlenbusch further

teaches the additional benefit of persistently turning devices on and off in a communication

10   system when not being used so as to conserve more power within the system (paragraphs 9 and

10).

It would have been obvious to one of ordinary skill of the art having the teachings of

Bongiorno, Kemeny and Ohlenbusch at the time the invention was made, to modify the clock

switching circuit of Bongiorno to include the ability to disable (power off) unneeded devices

15   when not in use as taught by Ohlenbusch such that when the back-up clock is powered on, the

unused detection circuit is powered off. One of ordinary skill in the art would be motivated to

make this combination of disabling (powering off) unneeded devices when not in use in view of

the teachings of Ohlenbusch, as doing so would give the added benefit of persistently turning

devices on and off in a communication system when not being used so as to conserve more

20   power within the system (as taught by Ohlenbusch above).

Response to Arguments

Applicant's arguments (in re independent claim 19) filed July 10, 2006 have been fully considered but they are not persuasive.

In re independent claim 19, Applicant argues that Bongiorno does not disclose a

5   processor and a means, wherein the means decouples without receiving any signal from the processor. Examiner respectfully disagrees. Bongiorno discloses an embodiment wherein the timer is connected to a microprocessor for detection purposes if the clock signal delivered to the microprocessor should become inadequate or fails (column 1, lines 10-32 and column 4, lines 9-21). Therefore, the embodiment does exist that comprises both a processor and a timer. The

10   means, shown above in claim 19, is the clock controller (40) which both detects whether a particular clock is available and couples/decouples those that are in case of failure. Furthermore, Bongiorno further discloses that the timer detects a clock failure, resets the processor and receives "programmed code" to further select which clock is best to couple to the processor (column 4, lines 9-21). Nowhere in Bongiorno is it disclosed that the means receives "a signal

15   from a processor" but merely that the clock controller (means 40) receives said programmed code.

Still in re claim 19, Applicant further argues that Bongiorno does not disclose a system clock input lead on the microprocessor. However, as shown above, it is inherent in the art that a processor chip will have a system clock input lead.

20   Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

5   A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

10   CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

Any inquiry concerning this communication or earlier communications from the

15   examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The

examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the

organization where this application or proceeding is assigned is (571) 273-8300.

20   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

James Sugent
5   Patent Examiner, Art Unit 2116
    September 21, 2006

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